TE EXTC C scheme Winter 2025 17/1/25

Duration: 3hrs [Max Marks: 80]

N.B. : (1) Question No 1 is Compulsory.
(2) Attempt any three questions out of the remaining five.
(3) All questions carry equal marks.
(4) Assume suitable data, if required and state it clearly.

Q1. Solve **any four** out of five **5**

a. Realize 4:1 Mux using pass transistor logic

b. Draw the circuit diagram of clocked S-R Flip flop using CMOS logic. **5**

c. Draw 4 *4 bit OR based array to store the following data in respective Memory locations.

Memory address	Data
1000	0011
0100	0101
0010	1010
0001	1101

d. Draw the VTC of CMOS Inverter and mark the various regions. **5**

e. What do you mean by Clock skew and Jitter explain in brief. **5**

Q2 Realize 2 – input NAND gate using CMOS logic **10**

a. a) Draw layout of realized circuit.

Find equivalent CMOS inverter for simultaneously switching of all input. Assume $\left(\frac{W}{L}\right)p = 20$, $(\frac{W}{L})n = 10$

b. Explain CMOS fabrication using the N-well process and discuss the CMOS latch-up problem. **10**

Q3 **10**

a Draw the circuit diagram of 3T DRAM memory and explain operation for reading and writing data into it. **10**

b Realize the expression Y= $\overline{(AB(C+D+E))}$ using the following logic style.

- CMOS logic
- Dynamic logic
- Pseudo Logic
- Domino Logic

Q4 **20**

a Design a 'FIR filter design' using the RTL design process. Also compare FSM with HLSM.

b Draw the block diagram of memory organization and explain the floating-gate transistor along with its role in flash memory.

Q5 **10**

a List the various types of capacitances present in a MOSFET. With the help of neat diagrams or cross-sectional views, explain each capacitance in detail. **10**

b What is the drawback of Binary ripple carry adder? Draw and explain the block diagram of Carry look ahead adder.

Q6 Write short notes on (any four)

a. Compare the effect of Full scaling and Constant voltage scaling on Current, Power, power density. State which is more power efficient **10**

b. Write short note on :(Attempt any TWO) **10**
1.Dynamic Logic
2.Carrry Select adder
3.Interconnect

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